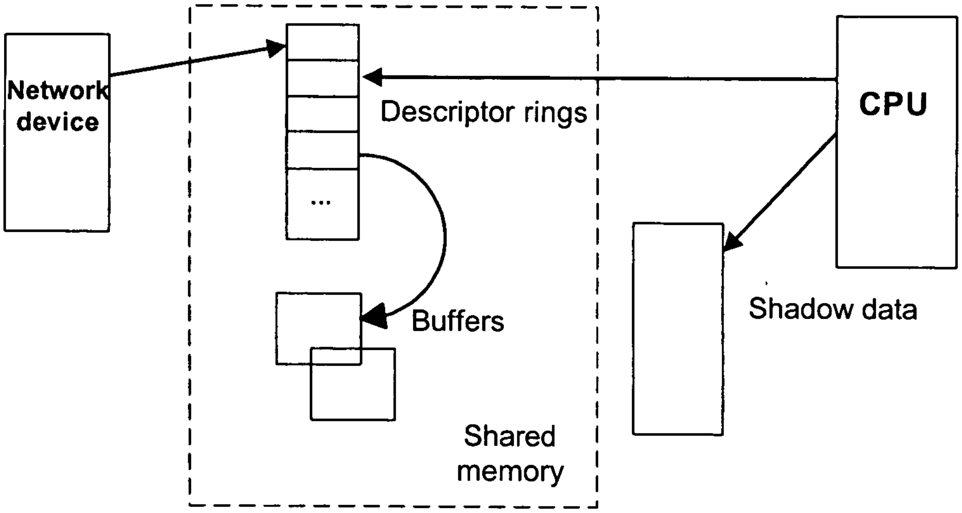

Network device
Descriptor rings
...
CPU
Buffers
Shadow data
Shared memory

Fig. 1

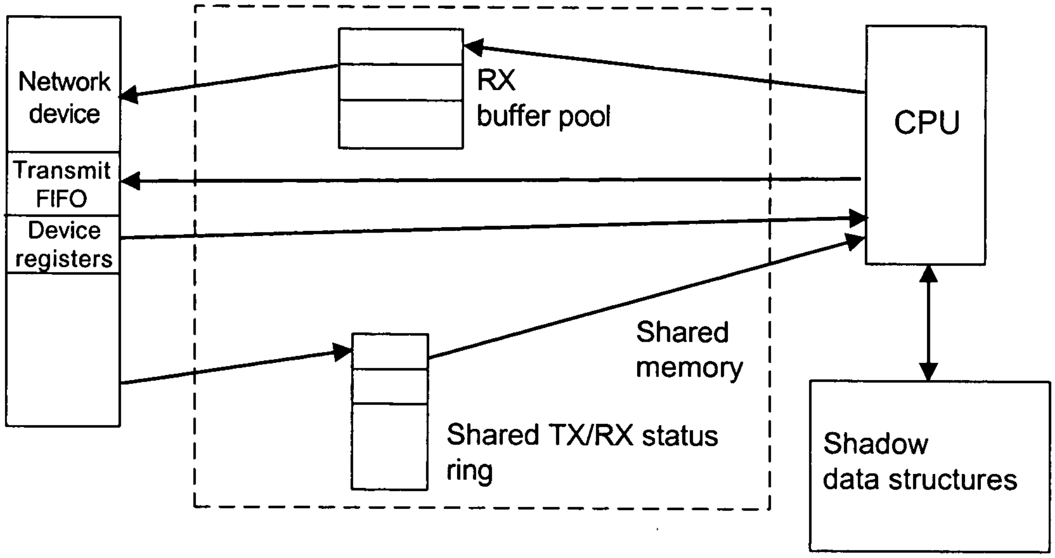

Network device
Transmit FIFO
Device registers
RX buffer pool
CPU
Shared memory
Shared TX/RX status ring
Shadow data structures

Fig. 2

Table 1: Data structure access

Resource	CPU	Device
RX Buffer pool	Write only	Read only
Status ring	Read only	Write only
TX FIFO	Write only	Internal resource
Device RX Registers	Write only	Internally maintained
Device TX Registers	Read only	Internally maintained

Fig. 3

Table 2: Device Registers

Register	CPU Access	Use
RX Buffer Count	Write only accumulator	Contains the count of the available buffers in the receive buffer pool.
Free Status Ring Entries	Write only accumulator	Contains the count of free status ring entries.
TX FIFO Free entries	Read only status	Contains the count of free transmit FIFO entries.

Fig. 4

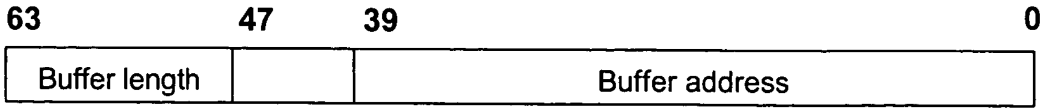


Fig. 5

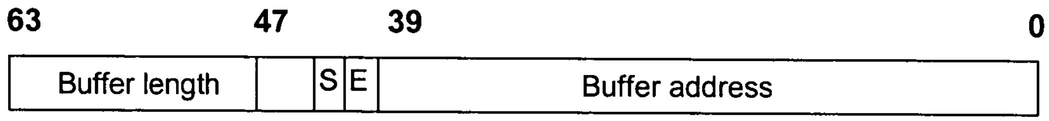


Fig. 6

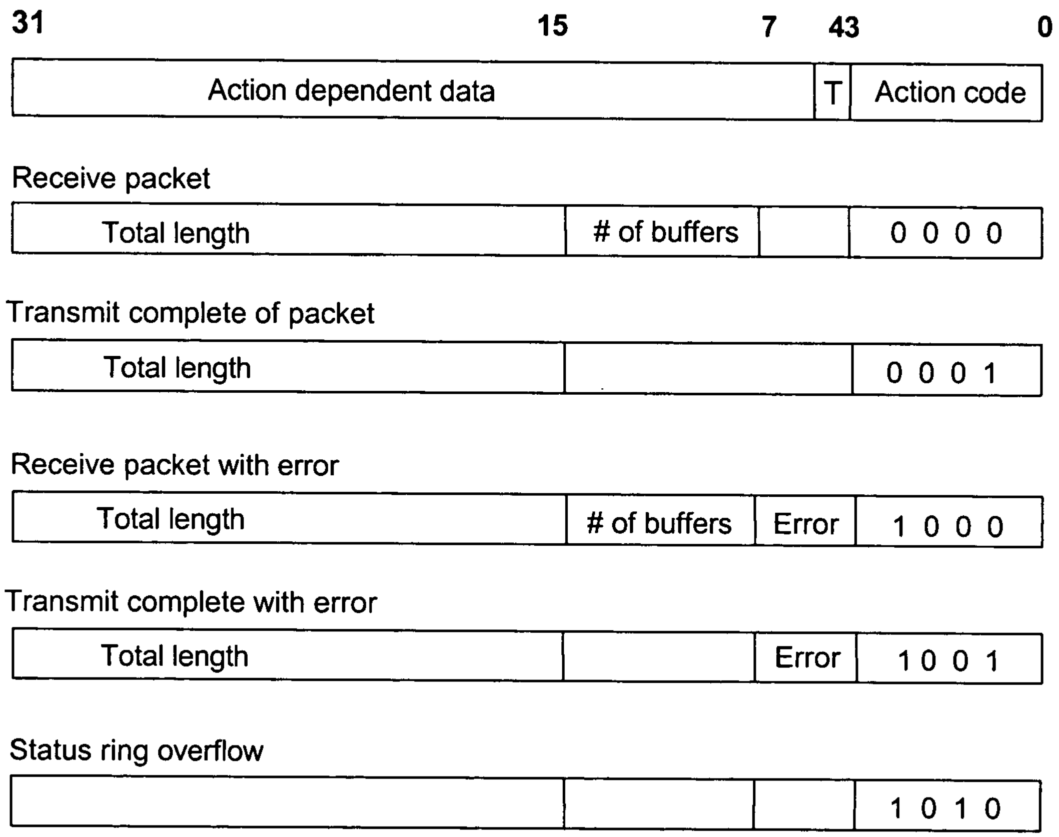


Fig. 7

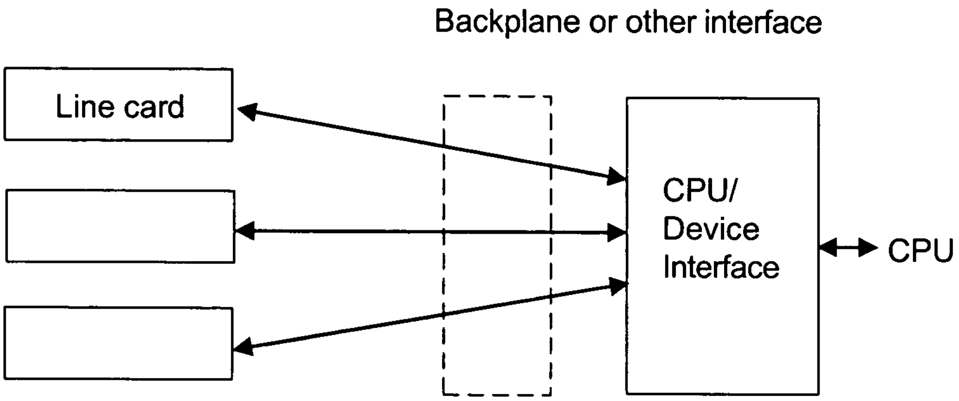

Backplane or other interface
Line card
CPU/ Device Interface
CPU

Fig. 8

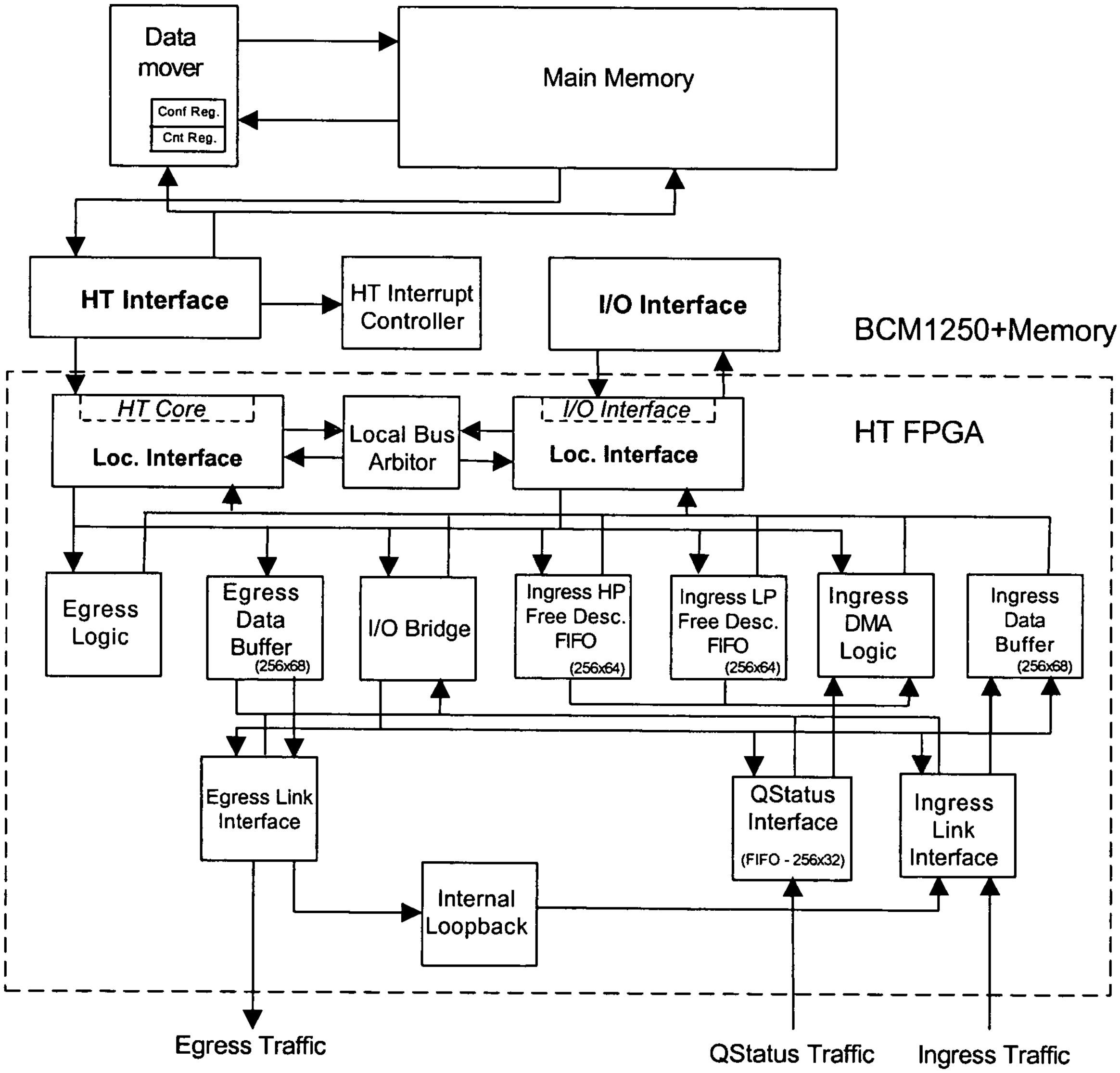

Data mover
Conf Reg.
Cnt Reg.
Main Memory
HT Interface
HT Interrupt Controller
I/O Interface
BCM1250+Memory
HT Core
Loc. Interface
Local Bus Arbitor
I/O Interface
Loc. Interface
HT FPGA
Egress Logic
Egress Data Buffer (256x68)
I/O Bridge
Ingress HP Free Desc. FIFO (256x64)
Ingress LP Free Desc. FIFO (256x64)
Ingress DMA Logic
Ingress Data Buffer (256x68)
Egress Link Interface
QStatus Interface (FIFO - 256x32)
Ingress Link Interface
Internal Loopback
Egress Traffic
QStatus Traffic
Ingress Traffic

Fig. 9

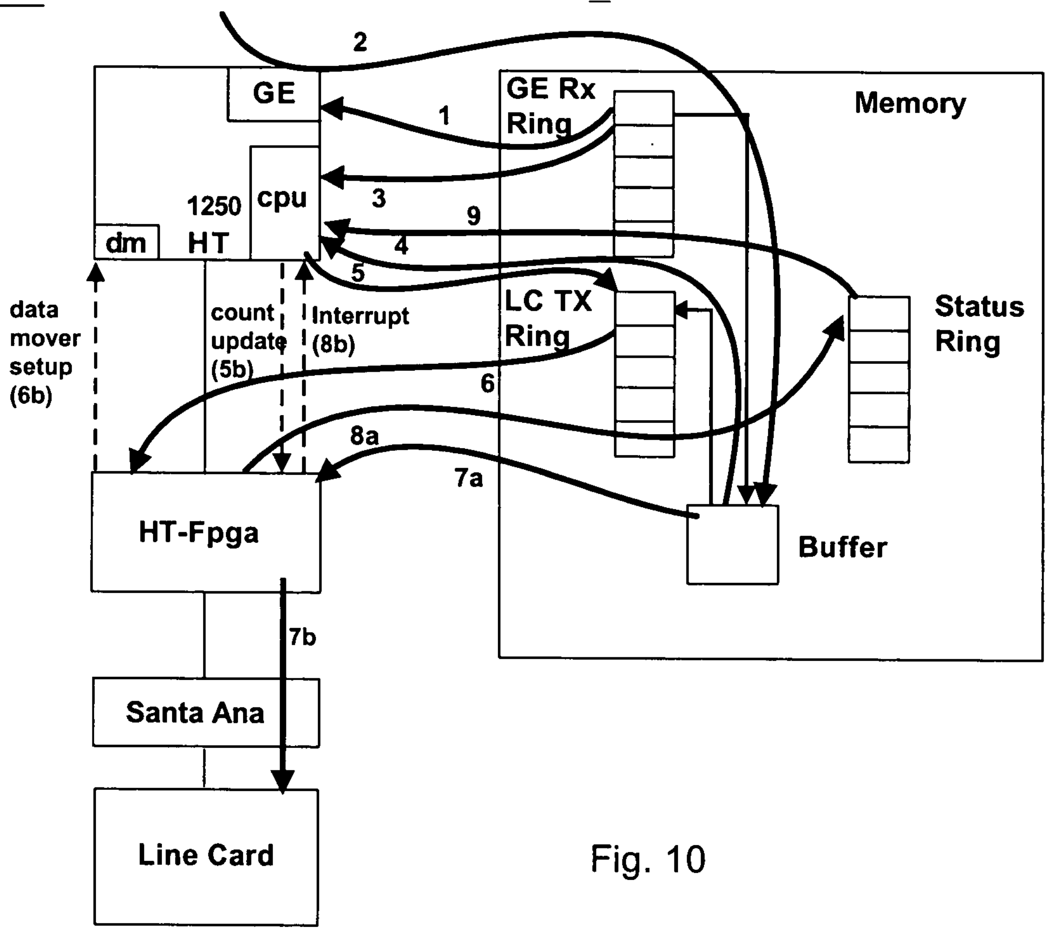
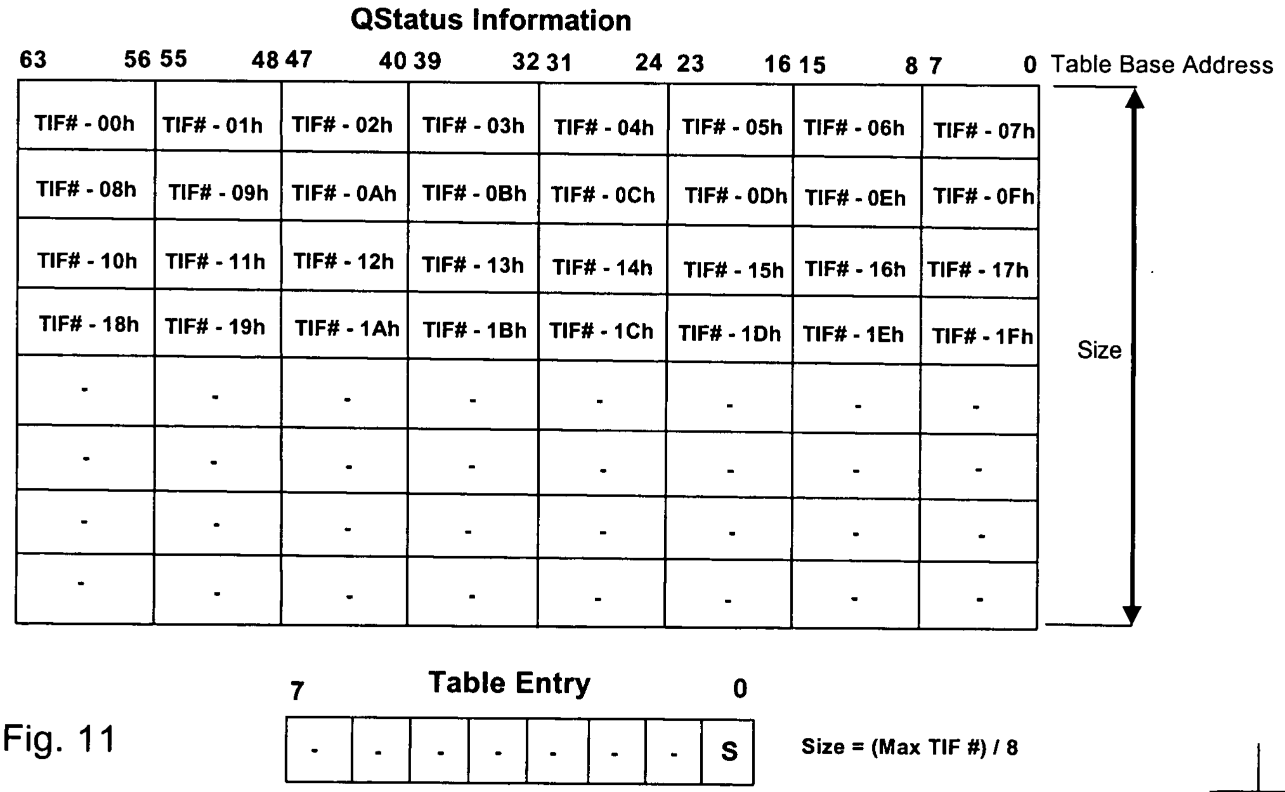


Fig. 10



QStatus Information

63 56	55 48	47 40	39 32	31 24	23 16	15 8	7 0	Table Base Address
TIF# - 00h	TIF# - 01h	TIF# - 02h	TIF# - 03h	TIF# - 04h	TIF# - 05h	TIF# - 06h	TIF# - 07h	
TIF# - 08h	TIF# - 09h	TIF# - 0Ah	TIF# - 0Bh	TIF# - 0Ch	TIF# - 0Dh	TIF# - 0Eh	TIF# - 0Fh	
TIF# - 10h	TIF# - 11h	TIF# - 12h	TIF# - 13h	TIF# - 14h	TIF# - 15h	TIF# - 16h	TIF# - 17h	
TIF# - 18h	TIF# - 19h	TIF# - 1Ah	TIF# - 1Bh	TIF# - 1Ch	TIF# - 1Dh	TIF# - 1Eh	TIF# - 1Fh	Size
-	-	-	-	-	-	-	-	
-	-	-	-	-	-	-	-	
-	-	-	-	-	-	-	-	
-	-	-	-	-	-	-	-	

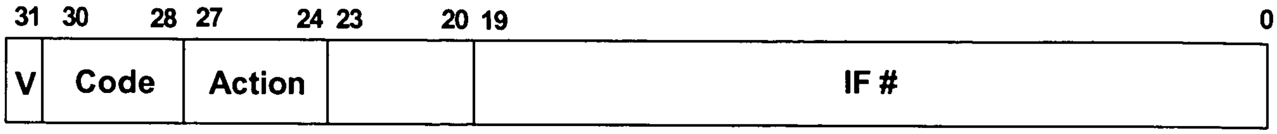
Table Entry

7							0
-	-	-	-	-	-	-	S

Size = (Max TIF #) / 8

Fig. 11

QStatus XON Entry Format



V = Valid bit, Code = 000, Action = *QStatus Code*, IF# = Interface Number

Fig. 12

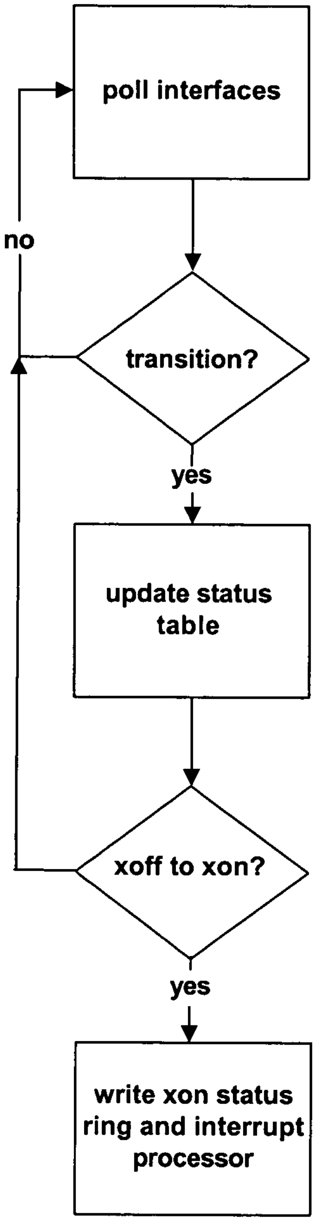


Fig. 13